REMARKS

The Office Action dated June 30, 2004, has been received and reviewed.

Claims 1-33 are currently pending and under consideration in the above-referenced application, each standing rejected.

Reconsideration of the above-referenced application is respectfully requested.

Preliminary Amendment

Please note that a Preliminary Amendment was filed in the above-referenced application on April 8, 2004, but that the undersigned attorney has not yet received any acknowledgement that the Preliminary Amendment has been entered into the Office file for the above-referenced application. If, for some reason, the Preliminary Amendment has not yet been entered into the Office file, the undersigned attorney would be happy to provide the Office with a true copy thereof.

Rejections Under 35 U.S.C. § 102

Claims 1-25, and 31-33 stand rejected under 35 U.S.C. § 102.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Ball

Claims 1-14, 16-25, and 31-33 stand rejected under 35 U.S.C. § 102(b) for reciting subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 5,291,061 to Ball (hereinafter "Ball").

Ball describes methods for assembling semiconductor devices in stacked arrangement to form relatively low-profile multi-chip modules (MCMs). In assembling the semiconductor devices, a "controlled-thickness . . . adhesive layer," which is formed from a thermoset material

(which is incorrectly referred to in Ball as a "thermoplastic" material) is formed between each adjacent pair of semiconductor devices. *See, e.g.,* col. 2, lines 63-65. Each adhesive layer has a minimized thickness that is "slightly greater than the low-loop wire [height], which is about 0.006 [inch]." Col. 3, lines 40-42. For example, the heights of the adhesive layers may be between 0.008 inch and 0.010 inch. Col. 3, lies 38-40.

Ball does not describe how the controlled-thickness adhesive layers are formed.

Independent claim 1 recites a method for forming an assembly that includes semiconductor devices in stacked arrangement. The method of independent claim 1 includes applying *substantially a predetermined volume* of adhesive material to an active surface of a semiconductor device. When a second semiconductor device is positioned adjacent to the first semiconductor device, the adhesive material spaces the second semiconductor device a predetermined distance apart from the active surface of the first semiconductor device.

Although Ball describes adhesive layers having specific thicknesses, Ball does not expressly or inherently describe that the adhesive layers may be formed by "applying substantially a predetermined volume of adhesive material to an active surface of a lower semiconductor device. In fact, Ball does not provide any description as to how the adhesive layers described therein are formed.

Accordingly, under 35 U.S.C. § 102(b), the subject matter recited in independent claim 1 is allowable over the subject matter disclosed in Ball.

Claims 2-14 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 4 is further allowable because Ball includes no express or inherent description of placing a semiconductor device on discrete conductive elements (*e.g.,* bond wires) that extend partially over a surface of another semiconductor device.

Claim 5 depends from claim 4 and is also allowable since Ball does not expressly or inherently describe introducing adhesive material between two semiconductor devices.

Claim 6, which depends from claim 5, is additionally allowable because Ball neither expressly nor inherently describes forcing the surface of one semiconductor device away from another semiconductor device.

Claim 7 also depends from claim 5, and is further allowable because Ball does not expressly or inherently describe substantially encapsulating portions of discrete conductive elements that are located over the active surface of a lower semiconductor device. Rather, as shown in the Figures of Ball, the adhesive layers thereof do not contact any portion of the bond wires described therein.

Claim 10 is additionally allowable since Ball lacks any express or inherent description of decreasing a distance the active surface of one semiconductor device is spaced apart from an opposing surface of another semiconductor device.

Claim 12 is further allowable since Ball does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Independent claim 16 is directed to a method for forming a multi-chip module. The method of independent claim 16 includes "applying substantially a predetermined volume of adhesive material onto at least a surface of [a] first semiconductor device . . ." A second semiconductor device is positioned over the first semiconductor device, with the adhesive material "spacing [a] surface of the second semiconductor device substantially a predetermined distance apart from the [an opposing] surface of the first semiconductor device."

Again, Ball does not include any express or inherent description of "applying substantially a predetermined volume of adhesive material" to the surface of a semiconductor device. Thus, Ball does not anticipate each and every element of independent claim 16, as would be required to maintain the 35 U.S.C. § 102(b) rejection of independent claim 16.

Each of claims 17-25 and 31-33 is allowable, among other reasons, for depending either directly or indirectly from claim 16, which is allowable.

Claim 19 is additionally allowable because Ball lacks any express or inherent description of applying adhesive material to a surface of a first semiconductor device after a second semiconductor device has been positioned over that surface.

Claim 25 is further allowable since Ball does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Claim 33 is also allowable because Ball lacks any express or inherent description of decreasing a distance the active surface of one semiconductor device is spaced apart from an opposing surface of another semiconductor device.

Fogal

Claims 1-14, 16-25, and 31-33 are rejected under 35 U.S.C. § 102(b) for being drawn to subject matter which is purportedly anticipated by the disclosure of U.S. Patent 5,323,060 to Fogal et al. (hereinafter "Fogal").

Fogal also describes MCMs. An MCMs according to Fogal includes an adhesive layer interposed between two semiconductor device that have been superimposed relative to one another. *See, e.g.,* col. 2, lines 13-18; col. 2, lines 49-54. The adhesive layer may be formed from an epoxy or an adhesive-coated tape. Col. 2 lines 67-68. The material may be electrically insulating. Col. 3, lines 8-9. The adhesive layer described in Fogal has a thickness (*e.g.,* 0.008 inch) that is greater than a loop height of bonding wires 44 that protrude above an active surface of the lower of the stacked semiconductor devices. Col. 2, lines 23-27; col. 2, lines 60-63; col. 3, lines 3-5.

Fogal does not provide any description as to how the adhesive layer described therein is formed.

With respect to the subject matter recited in independent claim 1, it is respectfully submitted that Fogal lacks any express or inherent description of "applying substantially a predetermined volume of adhesive material to an active surface of a first semiconductor device." Like Ball, Fogal makes no mention of how the adhesive layers described therein are formed.

Therefore, under 35 U.S.C. § 102(b), independent claim 1 recites subject matter which is allowable over that described in Fogal.

Claims 2-14 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 4 is further allowable because Fogal includes no express or inherent description of placing a semiconductor device on discrete conductive elements (*e.g.,* bond wires) that extend partially over a surface of another semiconductor device.

Claim 5 depends from claim 4 and is also allowable since Fogal does not expressly or inherently describe introducing adhesive material between two semiconductor devices.

Claim 6, which depends from claim 5, is additionally allowable because Fogal neither expressly nor inherently describes forcing the surface of one semiconductor device away from another semiconductor device.

Claim 7 also depends from claim 5, and is further allowable because Fogal does not expressly or inherently describe substantially encapsulating portions of discrete conductive elements that are located over the active surface of a lower semiconductor device. Rather, as shown in the Figures of Fogal, the adhesive layers thereof do not contact any portion of the bond wires described therein.

Claims 10 and 15 are additionally allowable since Fogal lacks any express or inherent description of decreasing a distance the active surface of one semiconductor device is spaced apart from an opposing surface of another semiconductor device.

Claim 12 is further allowable since Fogal does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Fogal likewise lacks any express or inherent description of "applying substantially a predetermined volume of adhesive material onto at least a surface of [a] first semiconductor device . . .," as required by independent claim 16.

As Fogal does not anticipate this element of independent claim 16, the subject matter recited in independent claim 16 is, under 35 U.S.C. § 102(b), allowable over the subject matter disclosed in Fogal.

Each of claims 17-25 and 31-33 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

Claim 19 is additionally allowable because Fogal lacks any express or inherent description of applying adhesive material to a surface of a first semiconductor device after a second semiconductor device has been positioned over that surface.

Claim 25 is further allowable since Fogal does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Claim 33 is also allowable because Fogal lacks any express or inherent description of decreasing a distance the active surface of one semiconductor device is spaced apart from an opposing surface of another semiconductor device.

Lin

Claims 1-25 and 31-33 have been rejected under 35 U.S.C. § 102(e) for being directed to subject matter which is assertedly anticipated by the subject matter described in U.S. Patent 6,333,562 to Lin (hereinafter "Lin").

Lin describes processes for separating the semiconductor dice of stacked multichip modules predetermined distances apart from one another. In these processes, conductive bumps 350 that include pillar protruding portions 350b are formed on bond pads of a lower semiconductor die 310. Col. 5, lines 9-14; FIG. 5; col. 6, lines 1-6; FIG. 8. An adhesive material is then introduced onto the active surface of the lower semiconductor die 310 to form an adhesive layer 340 thereon. Col. 5, lines 40-50; FIG. 7; col. 6, lines 23-28; FIG. 10. Another semiconductor die 320 is positioned over the lower semiconductor die 310, in contact with adhesive layer 340, and forced toward the lower semiconductor die 310 until the backside thereof contacts the pillar protruding portions 350b of bumps 350. *Id.*

In contrast to the subject matter described in Lin, independent claim 1 recites a method which includes "applying substantially a predetermined volume of adhesive material onto at least an active surface of a first semiconductor device . . .," which ultimately space the first semiconductor device apart from a second semiconductor device by substantially a predetermined distance.

Independent claim 16 is drawn to a method for forming a stacked MCM, which method includes "applying substantially a predetermined volume of adhesive material onto at least a surface of [a] first semiconductor device . . .," which ultimately results in the the surface of the first semiconductor device being spaced substantially a predetermined distance apart from an opposing surface of a second semiconductor device.

When the process described in Lin is employed, it does not matter how much (*i.e.,* the volume of) adhesive material that is applied to the surface of a semiconductor device. Rather, the pillar protruding portions 350b of the bumps 350 of Lin dictate the distance that two stacked semiconductor devices are spaced apart from one another. Therefore, Lin does not expressly or inherently describe applying "substantially a predetermined quantity of adhesive material" to a surface of a semiconductor device, as is required by independent claims 1 and 16.

As Lin does not anticipate each and every element of either independent claim 1 or independent claim 16, under 35 U.S.C. § 102(e), both of these claims recite subject matter which is allowable over the subject matter described in Lin.

Each of claims 2-15 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 4 is further allowable because Lin includes no express or inherent description of placing a semiconductor device on discrete conductive elements (*e.g.,* bond wires) that extend partially over a surface of another semiconductor device.

Claim 5 depends from claim 4 and is also allowable since Lin does not expressly or inherently describe introducing adhesive material between two semiconductor devices.

Claim 6, which depends from claim 5, is additionally allowable because Lin neither expressly nor inherently describes forcing the surface of one semiconductor device away from another semiconductor device.

Claim 7 also depends from claim 5, and is further allowable because Lin does not expressly or inherently describe substantially encapsulating portions of discrete conductive elements that are located over the active surface of a lower semiconductor device. Rather, as shown in the Figures of Lin, the adhesive layers thereof do not contact any portion of the bond wires described therein.

Claims 10 and 15 are additionally allowable since Lin lacks any express or inherent description of decreasing a distance the active surface of one semiconductor device is spaced apart from an opposing surface of another semiconductor device.

Claim 12 is further allowable since Lin does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Claims 17-25 and 31-33 are each allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

Claim 19 is additionally allowable because Lin lacks any express or inherent description of applying adhesive material to a surface of a first semiconductor device after a second semiconductor device has been positioned over that surface.

Claim 25 is further allowable since Lin does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Claim 33 is also allowable because Lin lacks any express or inherent description of decreasing a distance the active surface of one semiconductor device is spaced apart from an opposing surface of another semiconductor device.

Rejections Under 35 U.S.C. § 103(a)

Claims 26-30 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both

be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Fogal in View of Fujisawa

Claims 26-30 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Fogal, in view of teachings from U.S. Patent 5,801,439 to Fujisawa et al. (hereinafter "Fujisawa").

Each of claims 26-30 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

It is also submitted that Fogal and Fujisawa cannot be relied upon to establish a *prima facie* case of obviousness against any of the claims of the above-referenced application. Specifically, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fogal and Fujisawa in the manner that has been asserted.

The only possible motivation for one of ordinary skill in the art to combine the teachings of Fogal and Fujisawa would have been the fact that both references teach methods for stacking semiconductor devices. Nonetheless, the methods that are taught in Fogal and Fujisawa are completely different.

Fogal teaches stacked multi-chip modules that include bare semiconductor devices in stacked arrangement, as well as methods for assembling such multi-chip modules.

The teachings of Fujisawa are directed to packaged semiconductor devices with leads that extend along at least portions of the exterior surfaces of the molded packages thereof. These packaged semiconductor devices may be stacked relative to one another and secured to each other with adhesive material. Corresponding leads of adjacent packages contact and communicate with one another.

Moreover, neither Fogal nor Fujusawa teaches or suggests applying substantially a predetermined quantity of adhesive material to a surface of a semiconductor device so that it may be subsequently spaced substantially a predetermined distance apart from another semiconductor device, as required by all of the claims of the above-referenced application.

Therefore, it is apparent that the only source of motivation to combine the teachings of Fogal and Fujisawa would have been the disclosure of the above-referenced application, which would constitute improper hindsight.

In addition, it is respectfully submitted that neither Fogal nor Fujisawa teaches or suggests each and every element of any of claims 28-30.

With respect to claim 28, neither Fogal nor Fujisawa teaches or suggests that, when adhesive material is introduced between two semiconductor devices, discrete conductive elements that protrude from the active surface of one of the semiconductor devices are electrically isolated from an opposing surface of the other semiconductor device.

Fogal and Fujisawa also lack any teaching or suggestion that one semiconductor device may be pushed away from another semiconductor device as adhesive material is introduced therebetween, as required by claim 29.

Additionally, neither Fogal nor Fujisawa includes any teaching or suggestion that intermediate conductive elements may be coated with adhesive material as the adhesive material is introduced between two semiconductor devices.

For these reasons, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 26-30, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

Lin in View of Fujisawa

Claims 26-30 have also been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is allegedly unpatentable over the teachings of Lin, in view of the subject matter taught in Fujisawa.

Each of claims 26-30 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

In any event, a *prima facie* case of obviousness has not been established against any of claims 26-30. In particular, there would have been no motivation for one of ordinary skill in the art to have combined the teachings of Lin and Fujisawa in the manner that has been asserted.

The only possible motivation for one of ordinary skill in the art to combine the teachings of Lin and Fujisawa would have been the fact that both references teach methods for stacking semiconductor devices. Nonetheless, the methods that are taught in Lin and Fujisawa are completely different.

The teachings of Lin are limited to methods for stacking bare semiconductor devices.

The teachings of Fujisawa are directed to packaged semiconductor devices with leads that extend along at least portions of the exterior surfaces of the molded packages thereof. These packaged semiconductor devices may be stacked relative to one another and secured to each other with adhesive material. Corresponding leads of adjacent packages contact and communicate with one another.

Moreover, neither Lin nor Fujusawa teaches or suggests applying substantially a predetermined quantity of adhesive material to a surface of a semiconductor device so that it may be subsequently spaced substantially a predetermined distance apart from another semiconductor device, as required by all of the claims of the above-referenced application.

Therefore, the only motivation for one of ordinary skill in the art to combine the teachings of Lin and Fujisawa in the manner that has been asserted would have been derived from improper hindsight reliance upon the disclosure of the above-referenced application.

In addition, it is respectfully submitted that neither Lin nor Fujisawa teaches or suggests each and every element of any of claims 28-30.

With respect to claim 28, neither Lin nor Fujisawa teaches or suggests that, when adhesive material is introduced between two semiconductor devices, discrete conductive elements that protrude from the active surface of one of the semiconductor devices are electrically isolated from an opposing surface of the other semiconductor device.

Lin and Fujisawa also lack any teaching or suggestion that one semiconductor device may be pushed away from another semiconductor device as adhesive material is introduced therebetween, as required by claim 29.

Additionally, neither Lin nor Fujisawa includes any teaching or suggestion that intermediate conductive elements may be coated with adhesive material as the adhesive material is introduced between two semiconductor devices.

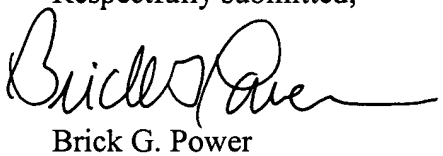
For these reasons, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 26-30, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 26-30 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1-33 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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